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**TECHNICAL PROGRAMS**

The following schedule lists highlighted conferences, symposia, standards workshops, and the like taking place during the San Francisco portion of this year's Semicon West. The general listings appear first, followed by the information for the SEMI Technical Symposium (STS) sessions. For a look at the San Jose programming or to check for the latest updates on the schedule of events, log onto SEMI's Web site, www.semi.org.

MONDAY, JULY 22**1–4 p.m.**

Stainless Steel and Surface Analysis Workshop

Marriott Hotel

Chairs: Sunniva Collins, Swagelok, GTA Welding Task Force; Tim Volin, Parker ICD, Surface Analysis Task Force

This standards workshop helps inform participants about the analysis of surfaces of components used in high-purity gas distribution systems for semiconductor manufacturing. There are presentations on test methods and results intended to measure corrosion resistance, contamination, and particulate generation in high-purity gas systems.

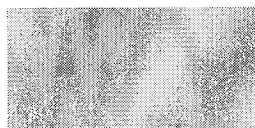
1–5:30 p.m.

STEP: 300-mm Wafer ID Mark— Requirements and Challenges

Marriott Hotel

Chair: Winthrop Baylies, Bay Tech Group

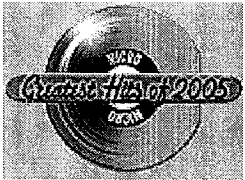
This Standards Technical Education Program (STEP) educates suppliers about the standard marked 300-mm wafers as well as the



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requirements suppliers face for reading and reporting wafer ID data. This program informs suppliers of their technical and schedule challenges and investigates what SEMI can do to assist both suppliers and users.

TUESDAY, JULY 23**8 a.m.–12:30 p.m.**

STEP: Practical Experiences with SEMI F47 Voltage Sag Immunity

Marriott Hotel

Chair: Cliff Greenberg, Nikon Precision

The new SEMI F47 standard sets requirements for how equipment must tolerate voltage sags on the ac power line. This program reviews the practical experience with this new standard as well as its associated testing standard, SEMI F42. Hands-on experience by test houses, subsystem suppliers, tool manufacturers, and semiconductor fabs is presented.

8:30–9:30 a.m.

European Union EHS Policy Briefing

Marriott Hotel

This briefing offers an overview of new and drafted legislation and regulations by the European Union in the environmental, health, and safety field that are relevant to the semiconductor industry. Topics include CE marking directives, future EU policy on chemicals, legislation on electrical and electronic equipment, and legislation on ozone layer-depleting substances and greenhouse gases.

8:30 a.m.–noon

Equipment and Materials Market Briefing

Moscone Center

Speakers: Sherry Garber, VP, Semico Research; Elizabeth Schumann, Director; Marketing and Research, SEMI; and Dan Tracy, Senior Market Analyst, SEMI

1:00–5:00 p.m.

Forecasting Techniques for the SEM Industry

Moscone Center

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Instructor: Moshe Handelsman, Advanced Forecasting

The course reviews major forecasting techniques used in the semiconductor equipment and materials industry, and their benefits and shortcomings. Forecasts of IC demand, wafer processing equipment sales, and test and assembly equipment sales for 2002 are presented and analyzed.

1:30–4 p.m.

Analytical Methods Workshop

Marriott Hotel

This workshop focuses on opportunities for online and offline analytical monitoring of processes and materials used in semiconductor manufacturing. Its purpose is to exchange information on how the semiconductor roadmap affects the analytical requirements for quality and quality control of materials. The workshop also provides an overview of analytical methods and how the information benefits semiconductor production.

Detection of Trace Impurities in Bulk Inert Gases Workshop

Marriott Hotel

Chair: Suhas Ketkar, Air Products and Chemicals

This workshop focuses on new advances in detection of trace (<1 ppb) impurities in bulk inert gases. Recent advances in analytical techniques have resulted in the development of lower-cost instruments to determine sub-ppb levels of H₂O and O₂ in bulk inert gases. Presentations in this workshop discuss new advances and provide insight into the use of those advances to monitor the quality of the supplied gases in real time.

3–5 p.m.

Developing a Highly Skilled Workforce in Your Company

Moscone Center

Instructor: Leonard Sledge, Manager of Education and Training Services, Maricopa Advanced Technology Center (MATEC)

The Maricopa Advanced Technology Center (MATEC) is a worldwide leader in education and industry collaboration, supporting the ongoing development of a highly skilled workforce for the semiconductor manufacturing industry, its suppliers, and customers. Partnering with SEMI and SIA, MATEC's program highlights electronically delivered

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training modules developed for trainers and designed for technician-level training.\

3–6 p.m.

EHS Interest Group Meeting—Life Cycle FAB Safety: Current Challenges and Solutions

Marriott Hotel

This meeting explores equipment throughout its life cycle in relation to protecting human safety and health. Each generation of equipment—from design through operating in a fab plant to decommissioning—challenges engineers and EHS professionals to improve the outcome. Topics such as global training issues, installation challenges, how design affects maintainability, and experiences with decontamination and decommissioning are explored.

6–8:30 p.m.

Standards Members Recognition Awards Reception

Marriott Hotel

WEDNESDAY, JULY 24

8:30 a.m.–5:45 p.m.

2002 International Technology Roadmap for Semiconductors (ITRS) Conference

Nikko Hotel

The draft International Technology Roadmap for Semiconductors (ITRS), 2002 update, is presented by each of the Technology Working Groups. Topics addressed include critical challenges, global technology requirements, areas for potential innovations, opportunities for audience feedback, and networking with ITRS working group presenters. Presentation sessions will be followed by an opportunity for feedback and questions from the audience. Lunch is provided. A reception follows the conference.

9 a.m.–5 p.m.

Understanding and Using Cost of Ownership

Marriott Hotel

Instructors: Wright Williams & Kelly

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This workshop explores how the semiconductor industry employs cost of ownership, providing a theoretical foundation and practical understanding of concepts and applications. With computer workstations, this lab-style workshop allows the participants hands-on experience in measuring COO sensitivities and examining their own equipment, materials, or fab conditions.

SEMI Technology Symposium (STS): Innovations in Semiconductor Manufacturing (all sessions held at the Marriott)

MONDAY, JULY 22

9 a.m.–noon

Session 101: Environmental, Health, and Safety (EHS) Part 1—
Treatment Technologies and Characterization Methodologies

Chairs: Laura Mendicino, Motorola; Sebastien Raoux, Applied
Materials; and Larry Zazzera, 3M

Advancements in Thermal/Wet Abatement of Low-k Process Effluents

Belynda Flippo, ATMI

Advances in Continuous Emissions Monitoring at Semiconductor
Fabs: The Implementation and Operation of a Multichannel FTIR-
CEM

Curtis T. Laush, URS

EHS Technology Transfer

David M. Hawkins, Intel

Equipment Risk Assessment Strategies and Tools: Five Case Studies

Sarah Bilimoria and Mary-j Klang, Applied Materials

Measuring and Modeling Gas Consumption and Emissions from
Semiconductor Manufacturing Processes

Rafika Smati, Applied Materials

Point of Use Abatement Analysis for Advanced CVD Applications

Laura Mendicino, Motorola Digital DNA Laboratories

Point of Use Treatment and Reclaim for Copper CMP/CMP
Wastewaters

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Richard E. Woodling, U.S. Filter

Reducing the Overall Environmental Impact of Low-k Processes

Joe Van Gompel, BOC Edwards

Session 102: Ramp Readiness

Chair: Sue Howell, SEMI

Industry experts discuss the legacy issues created during a downturn that have wreaked havoc on the ramp readiness capability of the supply chain. Topics include the components of a ramp readiness assessment, such as inventory, fixed costs, burden rates, and manufacturing flexibility. During the panel segment of the session, there is an opportunity to "ask the experts" about specific ramp issues. (Specific paper titles and presenters were not available at press time.)

Session 103: Gas Part 1—Gas Analysis

Chair: Virginia Houlding, Matheson Tri-Gas

An Investigation into the Use of Quadrupole Ion Trap Mass Spectrometry for the Analysis of Hydrocarbons in Inert Gases

Armando Colorado, Mykrolis

Detection of Nonstandard Impurities by APIMS in Semiconductor-Grade Nitrogen

Brian Warrick, Praxair

Determination of Moisture in Ammonia Using Negative Ion APIMS

Alan R. Bandy, Drexel University

Innovation in Gas Phase Purification and Analytical Techniques for Semiconductor Grade Ammonia

Barry Gotlinsky, Pall

Point-of-Use Sampling and Analysis for Metal Contaminants in Trichlorosilane

Dan Cowles, Air Liquide America—Balazs Analytical Services

Trace Impurity Detection in Ammonia for the Semiconductor Market

Suhas N. Ketkar, Air Products and Chemicals

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2-5 p.m.

Session 104: EHS Part 2—Addressing the Roadmap Challenges

Chairs: Larry Zazzera, 3M; Sebastien Raoux, Applied Materials; and
Laura Mendicino, Motorola

Beta Evaluation of a Plasma Exhaust Abatement System (Pegasys) of
Effluents from Etch Tools

Mohamed Alaoui, Applied Materials

Evaluation of MKS ASTRONex and C3F8 for Remote Plasma
Chamber Clean

Scott Bailey, ST Microelectronics

Addressing the Roadmap Challenges, Evaluation of C4F8O as an
Alternative Material in CVD Chamber Cleaning

David Harman, Intel

Evaluation of Perfluoroalkanesulfonyl (PFAS) Based Surfactants for
Semiconductor and Microelectronics Manufacturing

Michael J. Parent, 3M Specialty Materials Lab

Integrated Vacuum and Postpump Microwave Plasma Abatement
Solution Suitable for 300-mm Dielectric Etch and Other Processes

Jean-Christophe Rostaing, Air Liquide Centre de Recherche; Hervé
Dulphy, Air Liquide Electronics Systems; and Kenneth Caldwell,
Alcatel Vacuum Technology

Packaged On-Site Fluorine Generators for CVD Chamber Cleaning
Applications

Nancy C. Irwin, BOC Edwards

Quantification of the Environmental Impact of Photoresist and
Photoresist Residue with Supercritical Carbon Dioxide

Kimberly A Hershey, Praxair

Session 105: Innovations for Front End of Line Processes

Chair: Victor Ku, IBM

Evaluation of Various High-k Gate Dielectrics Using a Conventional

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MOSFET Process with Poly-Si Gate Electrode

Yudong Kim, International Sematech/Intel

Materials and Metrology Challenges for Silicon-on-Insulator (SOI) Wafers

Michael Ira Current, Silicon Genesis

Si/SiGe(C) Epitaxial Film Fabrication by a Single-wafer Cold-Wall UHVCVD System

Supika Mashiro, Anelva

Starting-Material Defectivity and its Impact on Yield in Silicon on Insulator (SOI) Devices

Richard Cuong Nguyen, AMD SDC

Systematic Development of Inorganic and Organometallic Precursors for Chemical Vapor Deposition (CVD)

Scott H. Meiere, Praxair

The 300-mm Era: New Challenges for SOI Production Equipment

Paul Lindner, EV Group

Session 106: Gas Part 2—Gas Delivery Systems

Chair: Jack Martinez, NIST

Corrosion Resistance of Cost-Effective Alternative Materials for Semiconductor Gas Distribution Systems

Joseph V. Vininski, Matheson Tri-Gas

Evaluation of Ceramic Filters Used in Ultra-High-Purity Gas Distribution Systems in Semiconductor Fabs

Holly Linkowich, Filterite Electronics

Purging Capability of Chemical Delivery Systems for Advanced CVD Precursors

Mindi Xu, Air Liquide

Status and Optimization of an Electronic Specialty Gas Distribution System Using a Mobile QC Cabinet

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Dmitry A. Znamensky, American Air Liquide

Streamlining Gas Delivery Systems Design and Management

Henry Hui, BOC Process Plants

Thermodynamic Considerations Of Liquefied Gas Container Head Space

David L. Ruppert, BOC Gases

TUESDAY, JULY 23

9 a.m.–noon

Session 107: Contamination-Free Manufacturing (CFM) Part 1—
Issues in Gas and Chemical Delivery

Chairs: Sowmya Krishnan, Ultra Clean Technology; and Ahmed
Busnaina, Northeastern University

Application of Point of Use Purifier for HCl on Multiple and Single-
Wafer Epitaxial Processes Giovanni Vaccari, MEMC Electronic
Materials

Contamination-Free Liquid Flow Controller

Chuck Gould, NT International

Metals Contamination From Chemical Filters Used for Semiconductor
Process Liquid and CMP Filtration

Thomas B. Gutowski, US Filter—Filterite Electronics

MFC Transient Response Relative to Gas Stream Pressure
Fluctuations and Set Point Changes

Gary D. Allen, Fugacity

Resist Stripping over Low-k Materials with Low-ion Plasma Processes
for Technologies Below 0.18 μm

Qingyuan Han, Axcelis Technologies

Session 108: Interconnect Part 1—Innovations in Interconnect
Technology

Chair: Neil Hendricks, ATMI

An Integrated Process Solution for

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sub-0.13- μ m Back-End Copper Interconnects

Michael Armacost, Applied Materials

Fast, Inline Copper Metrology Using Optoacoustics

Joshua Tower, Philips Analytical

Implementation of Plasma Processing Into BEOL with Organic Low-k Dielectrics

Robert Guerra, Mattson Technology

Multipurpose Ionized-PVD System Based on RF Plasma with Point-cusp Magnetic Field

Sunil Wickramanayaka, Anelva

The Pseudo-Leakage Current in Dual Damascene Tungsten CMP

Chung-Min Lin, Nanya Technology

2–5 p.m.

Session 109: CFM Part 2—Advanced Wafer Surface Preparation

Chairs: Sowmya Krishnan, Ultra Clean Technology; and Ahmed Busnaina, Northeastern University

0.18 μ m Solvent Clean Evaluation of 13 Different Chemistries Available

Danielle Kempa, National Semiconductor

Advanced 300-mm Wafer Surface Preparation Technologies to Address ITRS Requirements Matthew S. Lucey, SCP Global Technologies

Investigating Post-CMP Cleaning for STI Ceria Slurries

Robert Small, EKC Technology

Mechanical Interactions during Post-CMP Cleaning

Kristan G. Bahten, Rippey

Megasonic Particle Removal from Patterned Wafer Surfaces without Damage

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Jeffrey M. Lauerhaas, Verteq

Quantification Issues for the Measurement of Copper on Silicon Wafer Surfaces

Jiansheng (Jason) Wang, Air Liquide—Balazs Analytical Services

Standards for Molecular Contamination on Critical Surfaces in Cleanrooms

Daniel Robert Rodier, Particle Measuring Systems

Session 110: Interconnect Part 2—Technology for the 90 nm and Smaller Nodes

Chair: Rod Augur, Program Manager, Cu/Low-k Interconnect Integration, International Sematech

Challenges Associated with the Integration of Nanoporous Ultra Low k

Keith Buchanan

Establishment of a Baseline Flow at International Sematech Using Cu and Porous Ultra-low-k, Spin-on Dielectric

Rod Augur, International Sematech/Philips Semiconductors

Ultra Low keff Dielectric 90-nm and Smaller Nodes Challenges and Strategies

Brian Daniels, Honeywell Electronic Materials

WEDNESDAY, JULY 24

9 a.m.—noon

Session 111: The 300-mm Factory

Chair: Court Skinner, Factory Integration Technology Working Group, ITRS

AMS2000 ASIC Wafer Fabrication Realisation

Chris Buckland, Austriamicrosystems

Getting the Best 300-mm Fab Using the Right Design and Build Process

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Oded Tal, MAX International Engineering Group

How to Build an e-Diagnostics System

Peter Degen-Portnoy, Foliage Software Systems

Reducing Costs With the Farmed Fab Layout

Don Yeaman, M+W Zander; and Paul Stachura, Advanced Micro Devices

The Red Brick Wall: Finding Solutions to Factory Integration Challenges

Douglas Scott, PRI Automation

Vibration Impact of Tool Move-In Activities in an Operating 300-mm Fab

Ahmad Bayat, Vibro-Acoustic Consultants

Session 112: Innovations in Planarization Technology

Chair: Lily Yao, EKC

A Migration to Stress-Free Cu Polishing with Low-k and Ultra Low-k Dielectrics

Paul H. Yih, ACM Research

Cu CMP Slurry Evolution: Approaches to the Challenges of Cu/Low-k Integration

Jeff Chamberlain, Cabot Microelectronics

Development and Improvement of Abrasive Free Cu Polishing Slurry

Masanobu Hanazono, Hitachi Chemical

New Spectral Analysis Method to Quantify Nanotopography Impact on CMP

Jea-gun Park , Hanyang University

Research on a Novel Planarization Method as an Alternative to CMP

James E. Lamb, Brewer Science

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